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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,066	06/24/2003	Satoshi Matsuda	008312-0304355	1198

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EXAMINER	
TRAN, THIEN F	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/602,066	MATSUDA ET AL.	
	Examiner	Art Unit	
	Thien F. Tran	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,5,6,8,10,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,5,6,8,10,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 5, 6, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. (US 5,382,533) in view of Shell et al. (US 5,429,956).

Ahmad et al. discloses a semiconductor device (Fig. 2) comprising: (a) a semiconductor substrate (10); (b) a pair of first diffusion layers (26, 28, 44, 46) formed within said semiconductor substrate; (c) a gate insulating film including: (i) a first insulating film portion (12) formed on a portion of said semiconductor substrate which is positioned between said first diffusion layers, and (ii) a second insulating film portion (32 or 34) positioned on an edge of said first insulating film portion, said second insulating film portion having a thickness that is larger than a thickness of said first insulating film portion; (d) a gate electrode (18) having a first gate portion formed on the first insulating film portion (12) and a second gate portion formed on the second insulating film portion (32 or 34), in which the first and second gate portions are formed of the same material, an edge portion of the gate electrode side of each of the first diffusion layers being located outside of a side surface of the gate electrode; (e) a first gate side wall insulating film (30 of Fig. 2) formed on the side surface of said gate electrode (18) and on a side surface of said second insulating film portion (32 or 34), the first gate side wall

insulating film (30) having a first side surface and a second side surface, the first side surface being opposite to a side surface facing the gate electrode, the second side surface being opposite to a side surface facing the second insulating film portion, the first side surface being flush with the second side surface, and the first gate side wall insulating film (30) and the second insulating film portion (32 or 34) being formed of a same layer.

Ahmad differs from the claimed invention by not showing a second diffusion layer formed apart from said first diffusion layers within a portion of said semiconductor substrate which is positioned below said first insulating film portion.

Shell et al. disclose a second diffusion layer (40) formed apart from said first diffusion layers (60, 62) within a portion of said semiconductor substrate (10), which is positioned below said first insulating film portion (20) in Fig. 9.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to form a second diffusion layer apart from said first diffusion layers (26, 28, 44, 46) and positioned below said first insulating film portion of Ahmad et al. as taught by Shell in order to prevent punch-through in the channel region.

Regarding claim 5, Ahmad et al. in view of Shell discloses said first diffusion layers comprising a pair of extension regions (26, 28) formed below said gate side wall insulating film (30) apart from said second diffusion layer; and a pair of source-drain regions (44, 46) formed in contact with said extension regions (26, 28) on a side opposite said second diffusion layer.

Regarding claim 6, Ahmad et al. further discloses a second gate side wall insulating film (42) formed on a side surface of the first gate side wall insulating film (30).

Regarding claim 24, Ahmad discloses the same process step of thermal oxidizing the gate electrode and the gate insulating film. It is inherent that the bird beak regions (32, 34) characterized as a second insulating film portion have the same features as claimed, an upper surface of the second insulating film (32 or 34) is positioned higher than a top surface of the first insulating film portion (12), and a bottom surface of the second insulating film portion (32 or 34) is positioned lower than a bottom surface of the first insulating film portion (12).

Regarding claim 25, a distance between the first diffusion layers is longer than a gate length of the gate electrode.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. (US 5,382,533) in view of Shell et al. (US 5,429,956) as applied to claim 2 above, and further in view of An et al. (US 6,225,661).

Ahmad et al. in view of Shell et al. as described above does not disclose an interlayer insulating film formed to surround said first gate sidewall insulating film (30, 42) wherein an upper surface of said interlayer insulating film is coplanar with an upper surface of said gate electrode. However, it is old and well known in the art to form an interlayer insulating film surrounding said first gate sidewall insulating film (42) wherein an upper surface of said interlayer insulating film is coplanar with an upper surface of said gate electrode as shown for example by An et al. An et al. shows an interlayer

insulating film (40) surrounding a first gate sidewall insulating film (32), the interlayer insulating film having an upper surface being coplanar with an upper surface of a gate electrode (64). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to form an interlayer insulating film to surround said first gate sidewall insulating film (30, 42) wherein an upper surface of said interlayer insulating film is coplanar with an upper surface of said gate electrode as taught by An et al. in order to protect the gate electrode and the substrate from being contaminated and being shorted and to have the upper surface of the gate electrode exposed so voltage can be connected to the gate electrode for the transistor to be operational.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. (US 5,382,533) in view of Kim (US 6,472,284).

Ahmad et al. discloses a semiconductor device (Fig. 2) comprising: (a) a semiconductor substrate (10); (b) a pair of first diffusion layers (26, 28, 44, 46) formed within said semiconductor substrate; (c) a gate insulating film including: (i) a first insulating film portion (12) formed on a portion of said semiconductor substrate which is positioned between said first diffusion layers, and (ii) a second insulating film portion (32 or 34) positioned on an edge of said first insulating film portion, said second insulating film portion having a thickness that is larger than a thickness of said first insulating film portion; (d) a gate electrode (18) having a first gate portion formed on the first insulating film portion (12) and a second gate portion formed on the second insulating film portion (32 or 34), in which the first and second gate portions are formed of the same material; (e) a first gate side wall insulating film (30 of Fig. 2) formed on the side surface of said

gate electrode (18) and on a side surface of said second insulating film portion (32 or 34), and the first gate side wall insulating film (30) and the second insulating film portion (32 or 34) being formed of a same layer.

Ahmad differs from the claimed invention by not showing a second diffusion layer formed apart from said first diffusion layers within a portion of said semiconductor substrate which is positioned below said first insulating film portion; wherein a conductivity type of said second diffusion layer is opposite a conductivity type of said semiconductor substrate.

Kim discloses a second diffusion layer (307) formed apart from said first diffusion layers (310, 314) within a portion of said semiconductor substrate (300) of p-type, which is positioned below said first insulating film portion (301b); wherein a conductivity type (n-type) of said second diffusion layer (307) is opposite a conductivity type(p-type) of said semiconductor substrate.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a second diffusion layer (307) as taught by Kim into the structure of Ahmad so that the second diffusion layer is apart from said first diffusion layers (26, 28, 44, 46) within a portion of said semiconductor substrate (10) and positioned below said first insulating film portion (12); wherein a conductivity of said second diffusion layer is opposite a conductivity type of said semiconductor substrate (10) in order to control threshold voltage of the channel region.

Response to Arguments

Applicant's arguments with respect to claims 2, 5, 6, 8, 10, 24 and 25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F. Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thien F Tran

Thien F Tran
Primary Examiner
Art Unit 2811

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December 19, 2006